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(54) Adaptive optical sensor

(57) An efficient adaptivity to varying conditions of luminance is embodied in an optical sensor composed of an array of photosensitive cells each including a photosensitive structure, a storage capacitance, a first switch (CKSTORE) for storing the photogenerated charge in the capacitance, and a second switch (CKREAD) for selecting the capacitance when reading the charge stored therein, by detecting the level of the global current photogenerated by the totality of the photosensitive elements, during an initial phase of each frame capture, storage and reading cycle, and by subsequently controlling the closing interval of said first switch (CKSTORE) of the cells in function of the detected level of the global photogenerated current. The implementing control circuit may be realized in various forms.

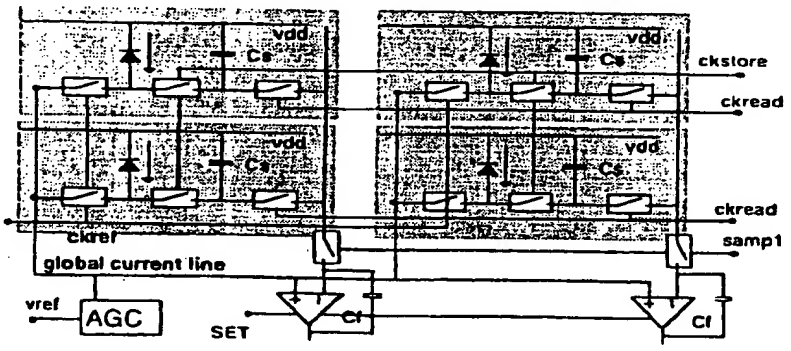

FIG. 2

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Description

The present invention relates to monolithically integrated image processing systems and more in particular to an adaptive optical sensor, monolithically integrated together with control and image processing circuitry.

Integrated optical sensors are becoming very useful in a number of application fields. Fundamentally, the sensor constitutes the image detector (video camera) in a certain format, for example in the QCIF format (176x144 pixels) and advantageously is monolithically integrated with the processing and control circuit. Integrated sensors of this type are useful in industry for realizing cameras suitable for functioning in hostile environments, for alarm and monitoring systems, for implementing of intelligent motion sensors and for filming in multimedia environments, PC, low OCR resolution, FAX and the like.

The following publications treat various aspects of the state of the art technology used for fabricating this type of optical sensors.

- "An Object Position and Orientation IC with Embedded Imager", David L. Standley, JSSC Vol. 26, n. 12 December 1991;
- "Smart Sensor Interface with A/D Conversion and Programmable Calibration", P. Malcovati, C. Azzeredo Leme, P. O'Leary, F. Maloberti and H. Baltes, JSSC Vol. 29, n. 8 August 1994;
- "A New MOS Imager Using Photodiode as Current Source", Mikio Kyomasu, JSSC Vol. 26, n. 8 August 1991;
- "Image Motion Detection Using Analog VLSI", Chu Phoon Chong, C. Andre, T. Salama and K.C. Smith, JSSC Vol. 27, n. 1 January 1992,
- "Smart Pixel Cellular Neural Network in Analog Current Mode CMOS Technology", S. Espejo et al., JSSC Vol. 29, n. 8 August 1994;
- "A 256x256 CMOS Active Pixel Image Sensor with Motion Detection", A. Dickinson, et al., ISSCC ISSN 0193-6530, February 1995, San Francisco.

The photosensitive portion of the integrated device is commonly constituted by an array or matrix of elementary cells, each corresponding to a pixel of a picked-up image (frame). The photodetector member of each cell may be a phototransistor or a photodiode. The luminous intensity of each pixel of an image optically projected over the area occupied by the array of photosensitive cells can be detected in terms of the current photogenerated by the photodetecting component of the respective cell.

The reading of an image detected by the array of photosensitive cells takes place by scanning in cyclic succession the cells, usually row by row. For each row of selected cells, the values relative to the single pixels of the row are commonly read in a parallel mode by a number of reading circuits equal to the number of pixels per row (i.e. equivalent to the number of columns of the photosensitive array). The values, read simultaneously for all the pixels of a selected row are "discharged" in a parallel mode, for example through a parallel-to-serial converter, in order to produce as output, a serial video signal including appropriate row synchronism pulses.

As an alternative to the use of phototransistors or photodiodes as photomodulated sources of a current proportional to the luminous intensity, which, adequately amplified, provides a pixel signal that may be sampled in the reading phase, stored and/or processed in various ways according to particular algorithms. The common use of a photodiode and of an associated capacitance that may be switched in parallel to the diode for a preestablished period of time for storing the value of luminous intensity of the respective pixel in terms of electric charge, has the advantage of allowing for a great simplification of the integrated structure of the individual cell.

Transfer of the charge photogenerated by the photodiode to the respective storing capacitance can be controlled by a dedicated integrated switch.

Normally, the subsequent reading destroys the information (pixel) temporarily stored in the cell capacitance, thus resetting the state of charge of the storing capacitance to a preset level. Therefore, the cell is ready again to record the next frame.

The reading of the state of charge of the capacitance is commonly enabled by a dedicated integrated read select switch, capable of coupling the storing capacitance of the cell (pixel) to the input of a charge amplifier, common for all the cells of a column of the cell array (that is, for pixels of the same order of all the rows).

A typical cell arrangement in rows and columns is shown in Fig. 1. The figure schematically illustrates the read select switches and the array of the reading charge amplifiers.

A frame is read selecting one row at the time in succession.

The pixel values, produced at the outputs of the charge amplifiers, for each selected row, are delivered in parallel

and converted into a serial signal by a dedicated parallel-to-serial converter circuit (not shown in the figure).

These systems require means for preventing saturation of the photosensitive elements (cells) and optimizing, that is adapting the sensitivity of the sensor to the illumination conditions of the scene or of the filmed subject. This requisite is of paramount importance because the variation of illumination between successive frames has a great impact on the global performances algorithm of analysis, principally based on the luminance component of the frames, especially so in the case of black and white videocameras.

Commonly, this function is electronically implemented through normal automatic gain control (AGC) loops, in function of luminance. A luminance signal can be generated in various ways. Often it is obtained from a dedicated sensor (exposure meter), integrated on the same device. In other systems, an average value of the frame luminance is obtained by processing the video signal itself. As a whole, the known systems rely on the controlling gain of a video signal amplifier, "downstream" of the sensor, through automatic gain regulation techniques.

These sensitivity regulation systems are intrinsically complex.

There is a need and/or utility of an "adaptive" sensor, capable of automatically implementing a control of its own sensitivity in function of the illumination level of the filmed subject, that is of the luminance of each frame without requiring the realization of burdensome signal processing circuits.

This aim is fully attained by the present invention whose object is a method and relative sensor's architecture, capable of exerting a sensitivity control of the optical sensor in response to the level of illumination of the subject or of the frame's luminance.

Therefore, control is implemented at each photogram (frame) by the sensor in an essentially adaptive way.

In a sensor operating in a cyclic mode and that stores each frame in the form of electric charge, the method of the invention consists of detecting, during a first phase of each cycle, the value of the global electric current resulting from the sum of the currents photogenerated by all the photosensitive elements that make up the sensor and in regulating the (shutter) closing interval of the switches through which the photogenerated current is integrated in the storage capacitance of each photosensitive cell, substantially in accordance with an inverse proportionality law in function of the preliminary assessed level of the global current.

The successive "reading" of the charge level of the storage capacitance, that corresponds to the relative intensity value of each pixel of the frame, eventually produces a video signal whose amplitude has already been adjusted on the ground of the frame's luminance level, without the need of further signal processing and compensation of the video signal.

According to an important aspect of the invention, this sensor adaptivity can be implemented with a particularly simple cell structure, realizable in a completely compatible way by a standard CMOS fabrication process, as it shown hereafter.

The processing circuitry of the global current and that for generating the appropriate control signals that establish the interval of integration of the current photogenerated in each photosensitive element, typically a photodiode, in its respective storage capacitance, in function of the preliminary measured global photogenerated current, can be realized in an essentially analog form or in an almost entirely digital form. Alternatively, its function can be partly implemented by processing via software an information relative to the global current in order to generate, via software, the desired time interval during which the frame's pixel values are stored as electric charge.

According to a fundamental aspect of the invention each individual cell comprises, in integrated form, beside its photosensitive structure, for example a photodiode, a storage (MOS) capacitance, a first switch for coupling the storage capacitance in parallel to the photodiode and a second read-select switch (discharge) for discharging the electric charge stored in the capacitance through the input of the charge amplifier (reading amplifier), also a third integrated switch. The latter has the function of connecting in parallel all the sensor photodiodes to a common line during an initial phase of each cycle. During this first phase of each cycle, the global current photogenerated by all the sensor cells is coupled, through a low impedance coupling circuit, to the input of a resettable charge amplifier. Therefore, the voltage ramp of the output node of the charge amplifier can be compared with a reference voltage by a comparator. The interval of time between the initial instant of a new cycle and the triggering of the comparator provides the primary information for enabling, based on other prearrangeable parameters, the closing time of the switch for integrating the photogenerated current of the photodiode its respective storage capacitance, thus implementing the desired adaptive function of the sensor to the changing illumination conditions, on a frame-by-frame basis. In practice, the system of the invention implements an automatic regulation of a parameter that can be equated to the exposure time (i.e. the shutter of a classical camera system). In other words, the invention realizes an electronic shutter whose opening time is automatically regulated in terms of illumination condition of the subject, on a frame-to-frame basis.

These and other aspects and advantages of this invention will be even more evident through the following description of some important embodiments and by referring to the enclosed figures, wherein:

Figure 1 shows, as previously mentioned, a typical organization of an array of rows and columns of photosensitive cells of a video sensor, each corresponding to a pixel of an image;

Figure 2 is a basic scheme of the cells of an adaptive sensor realized according to the present invention;

Figure 3 shows the timing diagrams for the adaptive sensor shown in Fig. 2;

Figure 4 is a layout of a single cell of an adaptive sensor according to the present invention;

Figure 5 is a block diagram of a videocamera realized according to the present invention;

Figure 6 is a diagram that shows the maximum "exposition" time that can be electronically determined by the adaptive automatic gain control system of the invention;

Figure 7 is a block diagram of an adaptive control circuit according to an embodiment of the invention.

The architecture of the single cells and their arrangement in an adaptive sensor realized according to the present invention is schematically shown in Fig. 2. In the partial scheme of this figure are illustrated four elementary cells and the respective scheme of electric connection during the different phases of each cycle of capture and storage of an image.

The diode symbol represents the photosensitive element of the cell, which includes also a storage capacitance Cs and three switches: CKREF, CKSTORE and CKREAD, respectively, which are controlled by the homonymous control signals. Among these, the CKREF signal controls, in common, the relative switches of all the cells that make up the sensor. The CKREF switches connect in common (that is in an OR configuration) all the photosensitive cells, that is the photosensitive elements, each constituted for example by a photodiode, to a unique line GLOBAL CURRENT LINE of photogenerated current. This common line, besides constituting an input of the block, generically indicates as AGC, of adaptive autoregulation of the sensor, is also coupled to a noninverting input of all the reading charge amplifiers (integrators) of the sensor to provide a common reference, identical to that of the cells.

All the CKSTORE switches are also commanded in common to close for a certain interval of time during which the photogenerated current in each photodiode is stored (integrated) as electric charge in the respective storage capacitance Cs, thus storing the image in the form of an electric charge.

By contrast, the read select switches of the cells are controlled, in sequence, row by row, by the control signal CKREAD. They allow the reading of the pixel value stored as electric charge in the capacitance Cs during the preceding frame storing phase, by coupling the capacitances Cs of the selected row of cells to the respective input lines of the reading charge amplifiers.

The scheme of Fig. 2 shows the employment of a switch SAMP1 on the read lines of the sensor. The use of such a switch is optional although highly preferable. Its function is that of preventing the integration of the charge due to the leakage currents. In fact, each read line has an intrinsic capacitance towards ground that is charged (or discharged) by the leakage current of the junctions of the devices that make up the CKREAD switches of the cells. It is important to prevent the integration of this leakage current on the reading charge amplifier when the signal on the integration capacitance C_f of the charge amplifier becomes available as output through a multiplexer. The switch SAMP1 isolates the read line from the input of the charge amplifier, preventing the leakage current to be integrated on the parasitic capacitance of the read line. By closing the switch SAMP1 the read line is properly "reset" before each reading phase (at each cycle). The switch SAMP1 is simultaneously closed during the reset phase of the reading charge amplifier and during the interval between successive switchings of the rows scanning signal CKREAD.

When all the three switches associated to each cell are p-channel devices, the control signal of the SAMP1 switches is a function of the logic signals CKREAD and SET:

$$\text{SAMP1} = \text{SET or } \overline{CKREAD}\,.$$

The relevant respective timing diagrams are shown in Fig. 3.

Fig. 3 represents a frame acquisition cycle by a QCIF format (176X144 pixels) camera.

During a first phase of the cycle identified as A in Fig. 3, reading of the global current generated by the sensor is performed by the automatic control circuit of the invention which produces a definition of the time interval of the successive phase B.

During phase B, the image is stored in the form of electric charge in the storage capacitance of the cells of the sensor. The charge of the storage capacitance occurs for an interval of time that is automatically determined by the control system during the preceding phase A.

During phase C the reset of the reading charge amplifiers and of the global current line takes place through the SET command and the successive reading of the charge stored in the various storage capacitances of the sensor through the CKREAD command. This is followed by the output of the read information through a parallel-to-serial conversion that is indicated identified in Fig. 3 as phase D. In the example considered, 144 of these successive phases C+D will

occur, in other words one for each sensor line. The total outputting time of the pixel signals is of 10.8 ms in the example considered.

At the end of the 144 C+D phases, all the pixel values so read and output the image (frame) acquisition cycle will be concluded and a new cycle may start. Each of new cycle of acquisition begins with a FSD (Frame Start Detector) pulse.

The layout of a single cell according to a particularly efficient form of integration is shown in Fig. 4. The shaded regions highlight the photodiode area, the area of the storage capacitance as well as the areas of the MOS devices that implement the three switches CKREF, CKSTORE and CKREAD which control the different phases of a cycle of operation of the cell.

These distinct phases of operation can by summarized according to the following table, where beside the state of the switches CKSTORE and CKREF, are also indicated, by way of an example, the respective timing intervals or preestablished limits of variation of the intervals, according to the requirements of the specific application of the sensor.

PHASE OF OPERATION	DESCRIPTION	CKREF	CKSTORE	TIME INTERVAL
Evaluation phase	Detection of the start FSD pulse of a new acquisition cycle and Start of the measuring of the photogenerated current	0	0	from 6.25 µs to 62.5 µs
Integration phase	Exposure interval (electronic shutter)	1	0	from 1.5 ms to 10.5 ms
Waiting phase	Waiting phase for a new frame acquisition cycle (FSD)	0	1	
Reset phase	A new FSD pulse resets the logic circuit and a new cycle begins at the next clock front	0	1	≈400 ns

Fig. 5 is a block diagram of a QCIF format (176x144 pixels) camera according to the present invention. The sensor is indicated by the 144x176 pels (pels=pixels) module, the SEQUENCER block represents the pixel scanning circuit of the sensor. The AMPLIFIERS block represents the array of the reading charge amplifiers. The PARALLEL-TO-SERIAL CONVERTER receives the output signals of the charge amplifiers and converts them in a serial signal that is made available at the ANALOG BUFFER output. The digital control circuit of the different phases is represented by the DIGITAL CONTROL BLOCK, whereas the circuit that implements the adaptive function of the invention is generically indicated as the AGC block.

Fig. 6 shows an operative diagram of the effects of the automatic control system of the "gain" of the optical sensor in function of the level of the global photogenerated current monitored during an initial phase of each cycle. In practice, the system of the invention that realizes an electronic shutter, has a first function that of establishing the maximum exposure time, in response to lower and lower illumination levels of the scene to be filmed.

Depending on the type of application of the sensor, such a maximum limit can be established in function, for example, of the ability of the human eye of perceiving images of increasing low luminance. This limiting function is easily implemented by defining a minimum threshold value of the global photogenerated current, that in the illustrated example of Fig. 6, may be 2µA, below which a maximum closing interval of the CKSTORE switches may correspond, so as to record an image in the form of electric charge stored in the storage capacitors Cs of the cells of the sensor, in a limit interval of about 10 ms.

Of course, if the sensor is to be used in certain image processing applications, for example in anticollision systems or in systems for preventing vehicles to go off course, where it is vital to ensure functionality of a real time analysis of the images picked up by the sensor even under very low luminance conditions (e.g. inside tunnels or during night traveling), such a minimum threshold can be lowered, consistently with the intrinsic signal to noise ratio characteristics of the photosensitive element or structure of the cells of the sensor.

As already mentioned, the system of the invention is based on a preventive estimate of luminance during a first phase of each frame acquisition cycle by sensing the level of the global current photogenerated by the whole array of photosensitive cells. The estimate of such a photogeneration level, directly tied to the irradiance of the filmed subject, may be realized by integrating the global photogenerated current on the integration capacitance of an appropriate charge amplifier, capable of producing a ramp signal whose gradient is representative of the level of the global photogenerated current.

Nevertheless, taking into account the relatively high capacitance of the lines, it is of paramount importance to ensure a coupling of very low impedance. Considering that the node is capable of picking up all the photogenerated current it has a considerable capacitance, it is fundamental that this node be a node of very low impedance to prevent deteriorating speed characteristics. Each photosensitive element loads this low impedance node with a capacitance that is the sum of the photodiode junction capacitance and of the storage capacitance. The sum of these two capacitances can be of about 500pF, which multiplied by the total number of cells, brings the value of the total capacitance to about 13nF. For these reasons it is highly recommendable to employ a dedicated coupling circuit between the node represented by the common current line to which all the photodiodes of the sensor are connected in an OR configuration through the respective CKREF switches, during the initial phase of each cycle.

Of course, any coupling circuit of low input impedance, known in the art, can be successfully used. A coupling circuit, particularly capable of providing a very low input impedance is described and illustrated in the article entitled: "The CMOS Negative Impedance Converter" by R. L. Brennan, T. R. Viswanathan and J. V. Hanson, IEEE Journal of Solid State Circuits, Vol. 23, No. 5, October 1988 (pages 1272-1275), whose content is herein incorporated by way of reference.

The circuit that processes the information relative to the illumination level of the scene provided by the gradient of the output ramp of a charge amplifier and generates a CKSTORE command whose duration is regulated in accordance with a law of inverse proportionality with the predetected level of the global photogenerated current, can be realized in different ways. As an alternative its function can be partially performed via software by arranging an analog-to-digital conversion of the primary information supplied by the charge amplifier of the global photogenerated current to provide a basic digital information that can be processed via software according to regulation criteria chosen by the operator.

An embodiment of the control circuit is shown in Fig. 7.

In the scheme of Fig. 7, the current generator Iph symbolically represents the whole sensor during a phase of OR connection of all the photosensitive elements through the respective CKREF switches to a unique output node through which is available the global photogenerated current.

The CURRENT DECOUPLER block has the function of providing a low coupling impedance with the output node represented by the common photogenerated current line. The input impedance of the CURRENT DECOUPLER block should have a value in the order of 10 ohms, and not higher than 100 ohms. The circuit described in the above mentioned article is perfectly fit for the purpose.

The global photogenerated current Iph is integrated by the resettable charge amplifiers CI1, whose output ramp drives the input node of a comparator COMP1 which switches at the instant in which the output voltage of the charge amplifier CI1 reaches a preestablished reference value. The voltage on the output node of the charge amplifier CI1, starting from a "reset" condition in which said output voltage can be for example 4V, drops with a ramp whose gradient, depending on the value of the integration (feedback) capacitance C1 may be in the order of 500pF, is proportional to the input current Iph. The reference voltage (triggering threshold) of the comparator COMP1 may be fixed at 1.5V, for example, so as to define a usable excursion range of 2.5V for the output voltage of the charge amplifier CI1.

The limit of adaptivity of the sensor, that is, of the automatic control system of the luminance may be established for example by "duplicating" the circuit constituted by the charge amplifier and by the comparator and by feeding the input of the second resettable charge amplifier CI2 having an integration (feedback) capacitance C2 of about 5pF, a preestablished current Iref, through a common adjustable current generator, equivalent to the minimum threshold of global photogenerated current that should be preestablished for inhibiting the adaptive capacity of the sensor below a certain minimum level of irradiance of the filmed subject.

The output of the two comparators COMP1 and COMP2 are combined in OR by means of a dedicated logic gate so as to provide a logic step command of the reading phase of the level of the global photogenerated current to a logic control circuitry. The logic control block receives the pulse start (FSD) of a new frame acquisition, storage, and reading cycle, a timing signal CLOCK and a reset command of all the reading charge amplifiers as well as of the charge amplifiers CI1, CI2 and CI3 of the control circuit and of any other device that must be reset to a certain state before carrying out a new working cycle such as the state of the comparators COMP1, COMP2 and COMP3. The control circuit generates the control phase CKREF, as well as the control signal of the RESET switches and of the switches that select the input currents Irs and Irf of the double ramp generator, thus producing the regulated phase CKSTORE that controls the closing of the frame storage switches of the cells of the sensor.

The closing command for a regulated interval of time of the switches CKSTORE can be produced, according to the embodiment of Fig. 7, by employing a double ramp generator realized by a third charge amplifier CI3, onto the input node of which a first reference current Irs and a second reference current Irf of opposite sign may be switched. The output of the charge amplifier CI3 drives the input of a third comparator COMP3 of the hysteresis type capable of supplying respective logic commands to the control logic circuit.

The functioning of the circuit of Fig. 7 can be described by referring to the functioning phases indicated in the table already shown above.

ESTIMATION PHASE OF THE INTEGRATION INTERVAL (TDP)

The global photogenerated current Iph is read by the decoupling block CURRENT DECOUPLER, which supplies a low resistive type impedance, lower than 100 ohms. The current is integrated by a charge integrator CI1 which starts from a condition whereby its output level has been reset to 4V. The integrated current will tend to lower the output voltage until it reaches a reference voltage for example of 1.5V. In practice, the integration interval of the current generated by the photodiodes is proportional to the time required by the output level of the amplifier CI1 to go from a voltage of 4V to a voltage of 1.5V. It is important to point out that this interval of time is inversely proportional to the total photogenerated current Iph. By calling C1 the integration capacitance and knowing that the output voltage swing of the amplifier is of 2.5V, the time taken by the amplifier to accomplish such an excursion can be obtained with the following equation:

$$T=2.5*C1/Iph \quad [1]$$

The output voltage of the charge amplifier CI1 commands the comparator COMP1 that triggers when its input (+) drops below 1:5V.

During this phase, the S3 switch is closed and the current Irf delivered by the amplifier CI3, tends to rise the output voltage of CI3 until the comparator COMP3 triggers.

INTEGRATION PHASE

During this phase, CI1 is in a stand-by condition. The switch S3 opens while S4 closes. In this precise instant the output voltage (V3) of CI3 is exactly equal to V3=Vref(1.5V)+T*Irf/C3 which, considering equation [1], becomes V3=Vref+2.5*C1*Irf/(C3*Iph) .

The current Irs has an opposite sign of Irf thus V3 drops with a gradient given by Irs/C3. This continues until V3 becomes equal to Vref thus the hysteresis comparator COMP3 triggers, generating a logic signal which indicates to the control logic that the integration phase is completed.

The duration of the integration phase is therefore equal to the time T multiplied by the ratio Irs/Irf, so that possibility for regulating the integration time consists in changing the ratio between these two currents.

In reality, the comparator COMP3 triggers at a slightly lower voltage due to the fact that the comparator is provided with a hysteresis (for example of about 50mV) which is introduced for preventing possible oscillation phenomena when the input level remains in the vicinity of the reference voltage Vref.

There exists the problem, under conditions of scarce illumination, that the integration time be expanded beyond the allowable limit (it should be remembered that the exposure time should be inversely proportional to the average total radiant power). Therefore, a maximum limit of this interval, is introduced by employing an amplifier CI2 identical to CI1, controlling a respective comparator COMP2, into which a reference current Iref in injected that triggers the comparator COMP2 after a certain maximum interval of time that may be fixed by adjusting the injected current. An OR gate triggers when one of the two comparators (no matter which) triggers. In general, under sufficient or high illumination, the comparator COMP1, controlled by CI1, will trigger while under scarce illumination the comparator COMP2 controlled by CI2 will trigger so as to establish a limit to the adaptivity of the sensor below a certain minimum level of illumination.

Of course, the current Irs and Irf can also be generated by constant current generators that may be regulated for defining the law of dependency of the closing time of the CKSTORE switches from the global current level Iph, as measured during the first phase of each new frame acquisition cycle.

As it will be obvious to a person skilled in the art, the adaptive automatic control circuit of this invention can also be realized in a different way from that described in relation to the scheme of Fig. 7. For example, the automatic control circuit can be realized in a purely digital form instead of in an analog form as shown in Fig. 7. The information relative to the detected level of the global photogenerated current, can be digitized and in this form digitally processed so as to obtain a control phase that determines the duration of the integration time of the frame in the form of electric charge, in function of parameters set by the operator.

Claims

1. Method of adaptive control of the sensitivity of an optical sensor comprising an array of photosensitive elements, each associated to a storage capacitance for the photogenerated current, a first switch (CKSTORE) for storing of the photogenerated charge in said capacitance and a second switch (CKREAD) for selecting said storage capacitance to read the charge stored therein, characterized in that it comprises

   detecting during a first phase of each capture, storage and reading cycle of a frame the level of a global current photogenerated by the totality of said photosensitive elements;

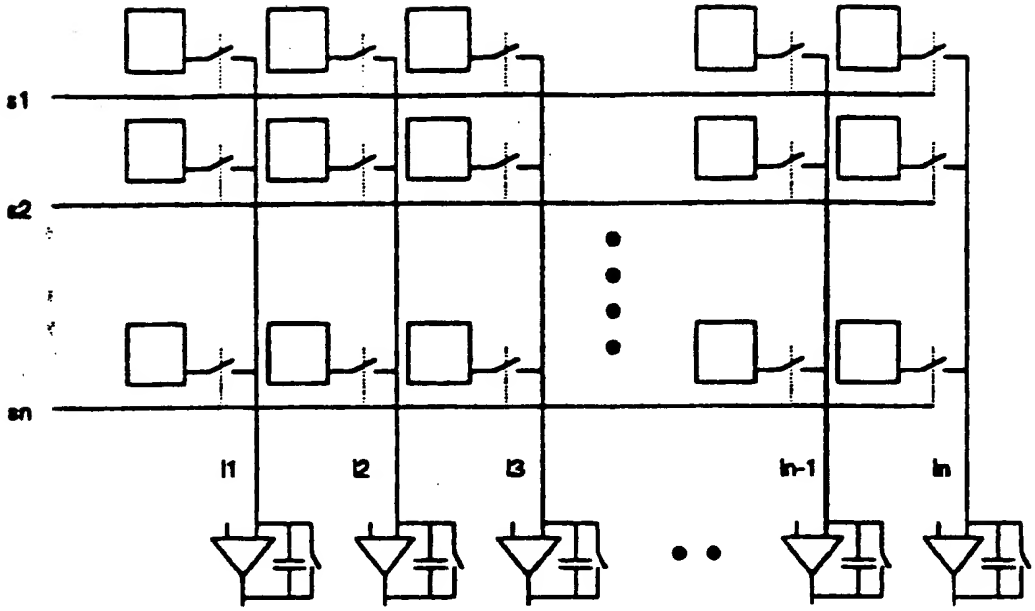

s1
s2
sn
I1
I2
I3
In-1
In

FIG. 1

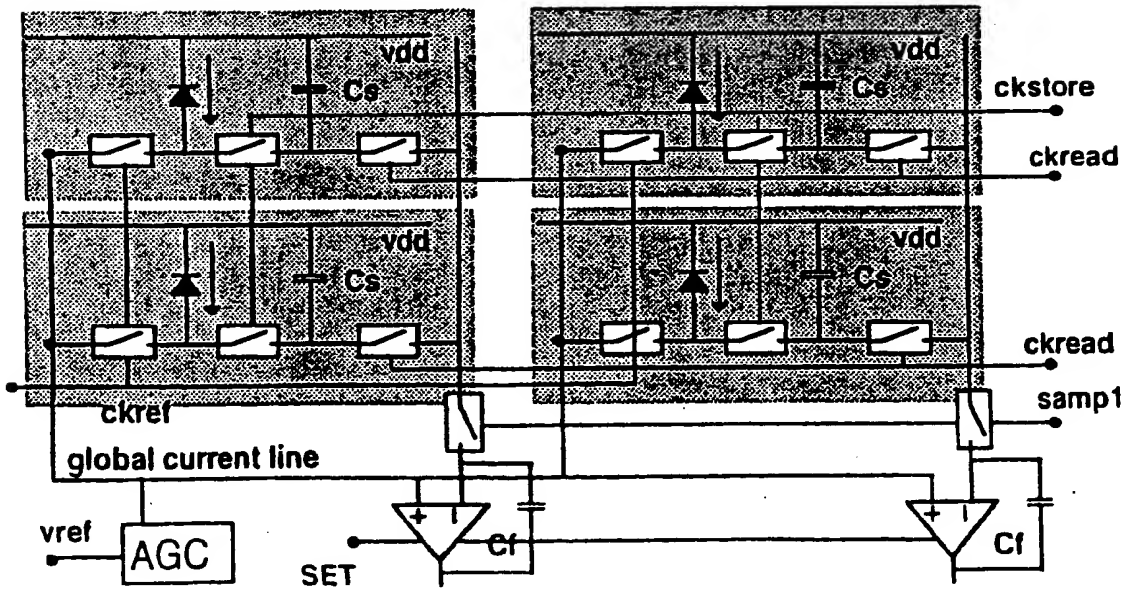

vdd
Cs
ckstore
ckread
ckread
samp1
ckref
global current line
vref
AGC
SET
Cf
Cf

FIG. 2

controlling the closing interval of said first switches (CKSTORE) in function of the level of said global current during a phase following said first phase.

2. The method according to claim 1, characterized in that it comprises establishing a minimum threshold value of the level of said global photogenerated current from the totality of said photosensitive elements corresponding to a maximum time interval of closing of said first switches (CKSTORE).

3. The method according to claim 1, characterized in that control of the closing interval is implemented in an automatic manner.

4. The method according to claim 1, characterized in that control of the closing interval is implemented via software.

5. An adaptive optical sensor comprising an array of cells, each comprising a photosensitive element, a first switch (CKSTORE) for storing the current photogenerated by the photosensitive element in a respective storage capacitance (Cs) and at least a second switch (CKREAD) for selectively reading the charge stored in said capacitance (Cs) during a frame reading scan of said array,

characterized in that

each cell comprises a third switch (CKREF), driven in common to that of all the other cells of the array for connecting in an OR configuration all said photosensitive elements to produce a global photogenerated current (Iph);

timing means capable of configuring said switches (CKREF, CKSTORE, CKREAD) during distinct phases of each frame capturing, storing and reading cycle;

means capable of regulating the closing interval of said first switches (CKSTORE) in function of the level of said global photogenerated current (Iph), detected during a first phase of each cycle.

6. The adaptive optical sensor according to claim 5, characterized in that said photosensitive element is a photo diode.

7. The adaptive optical sensor according to claim 5, characterized in that said means regulating the closing interval of said first switches (CKSTORE) comprise at least a low input impedance circuit (CURRENT DECOUPLER) coupling a common node, to which are connected in OR all said photosensitive elements, to the input of a first resettable charge amplifier (CI1) whose output drives a first comparator (COMP1) capable of generating a logic signal representative of the level of said global photogenerated current (Iph);

a second resettable charge amplifier (CI2) to an input of which a first reference current (Iref) is applied and whose output drives a second comparator (COMP2) capable of generating a second logic signal representative of a preset minimum limit of the level of said global photogenerated current (Iph);

a double ramp generator comprising a third resettable charge amplifier, to an input of which are alternately switched a second (Irs) and a third (Irf) reference current of opposite signs, and whose output drives an hysteresis type third comparator (COMP3) capable of generating a third logic signal;

a timing control circuit receiving as input a start impulse (FSD) of a new cycle, a reset command (RESET) and a timing signal (CLOCK) and controlling reset switches of said charge amplifiers, selection switches of said second (Irs) and third (Irf) reference currents and generating control phases of said first (CKSTORE) and third (CKREF) switches of the cells.

8. A videocamera characterized in that it includes an adaptive optical sensor in accordance with claim 5.

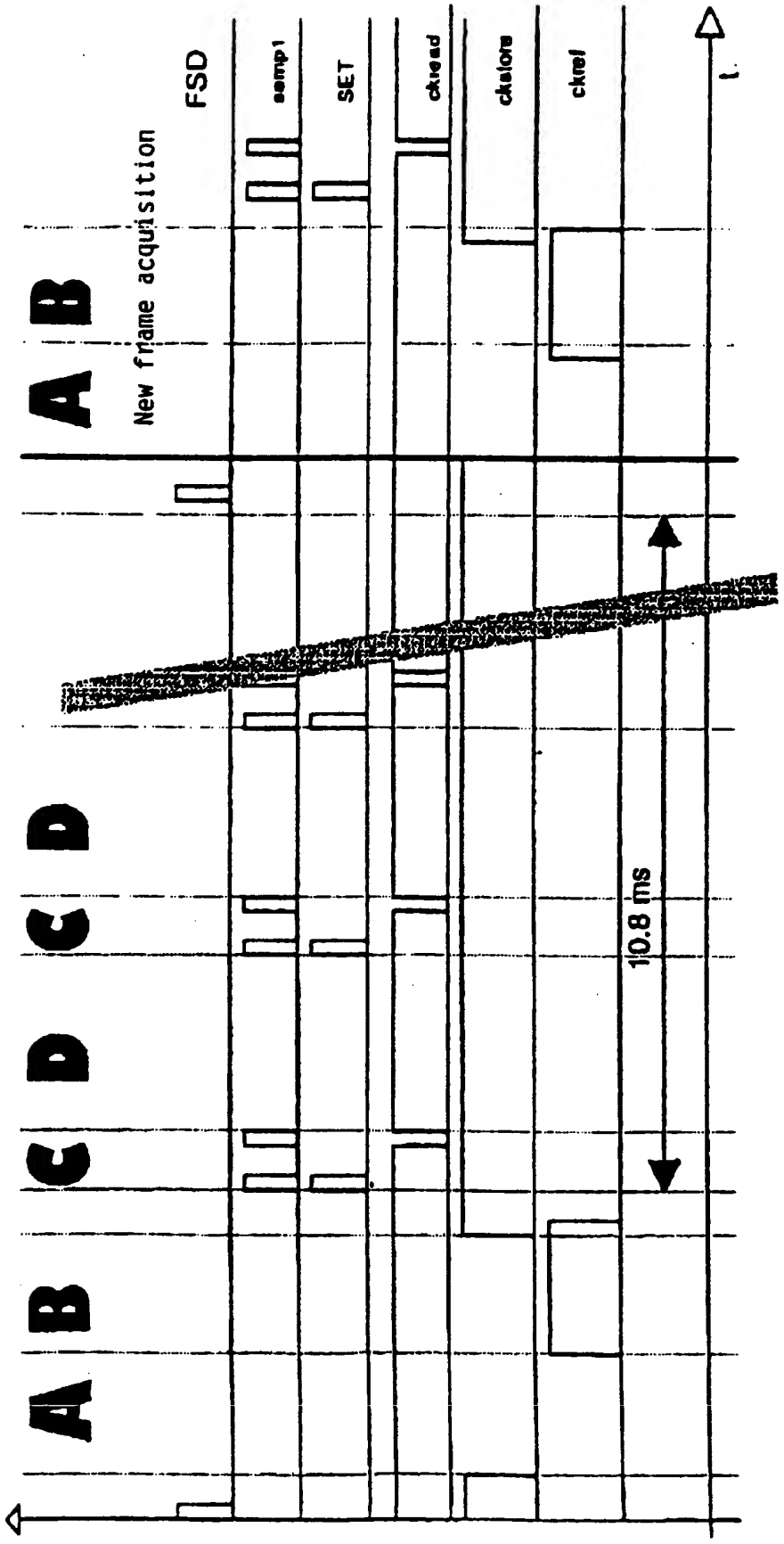

A B
New frame acquisition
FSD
sampl
SET
ckread
ckclone
ckrel
t
A B C D C D
10.8 ms

FIG. 3

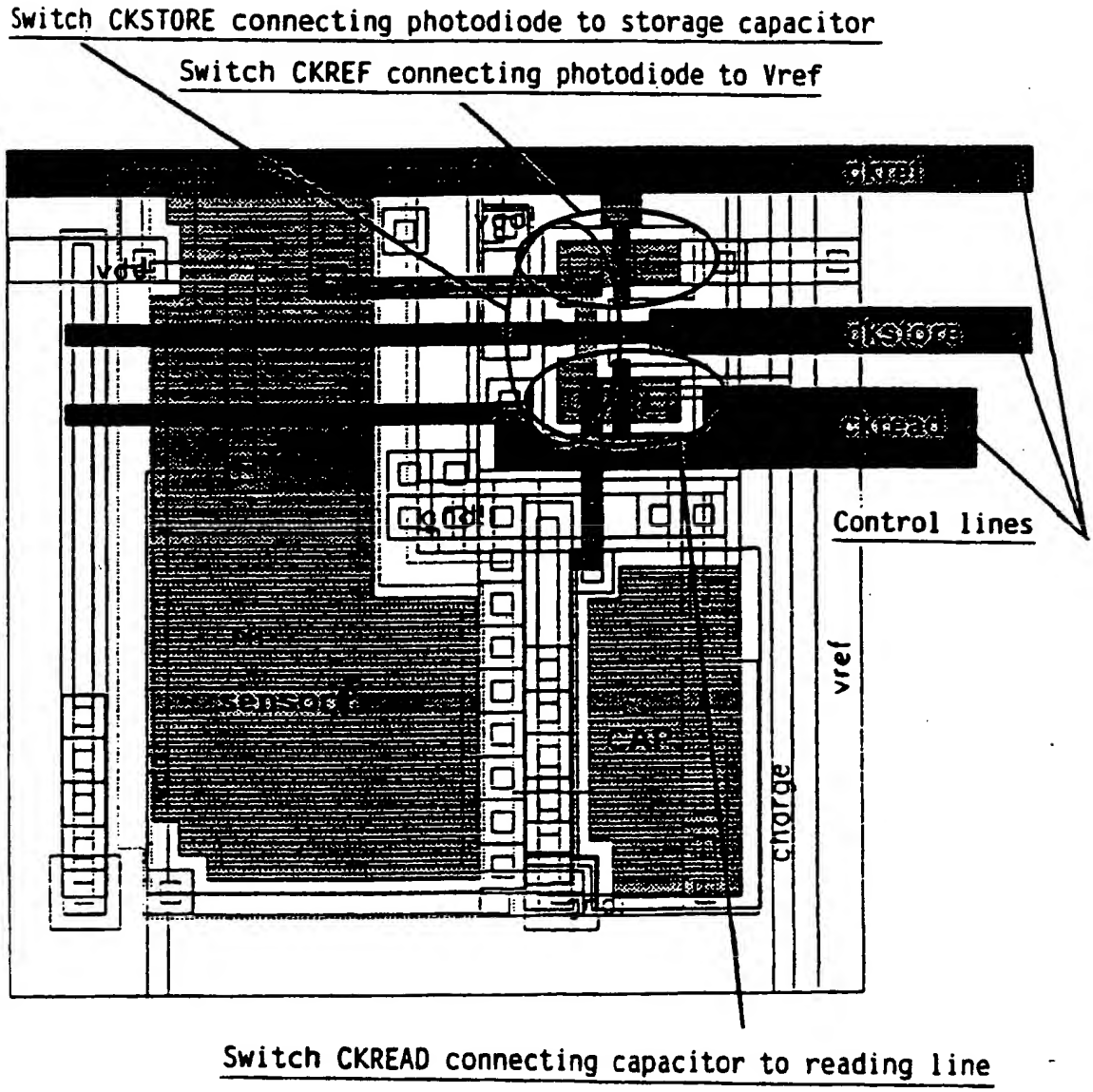

Switch CKSTORE connecting photodiode to storage capacitor
Switch CKREF connecting photodiode to Vref
Control lines
vref
charge
Switch CKREAD connecting capacitor to reading line

FIG. 4

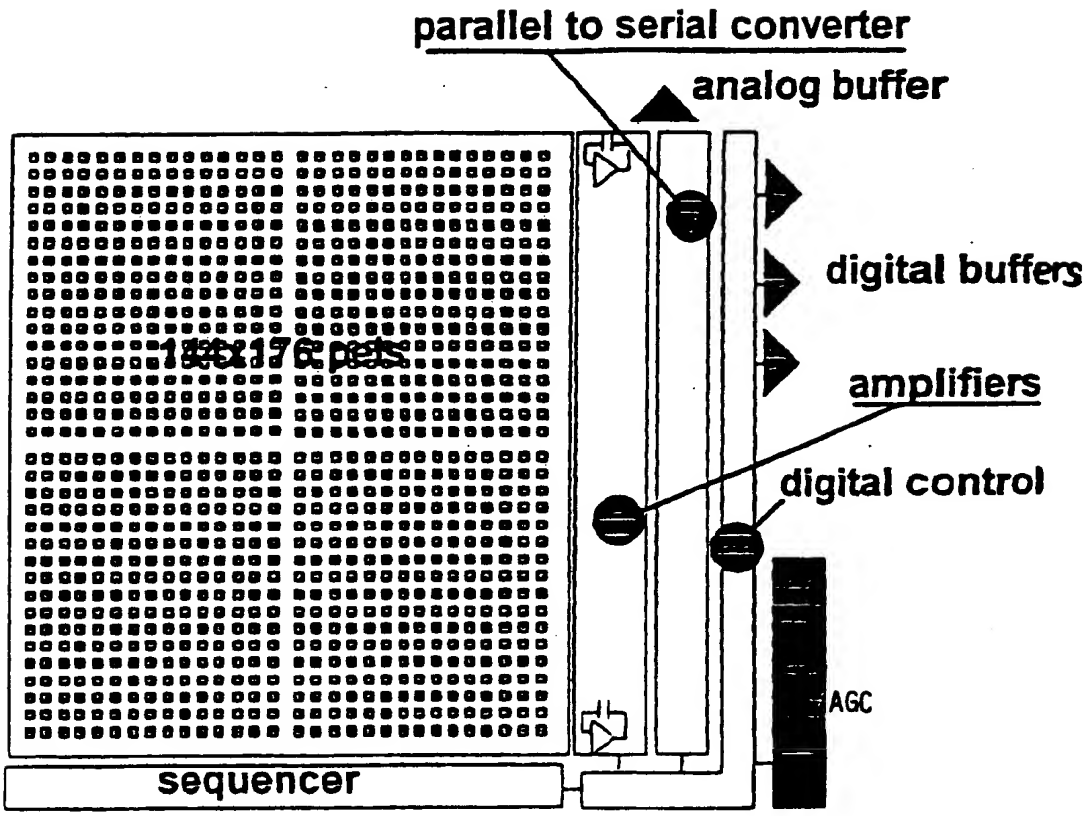
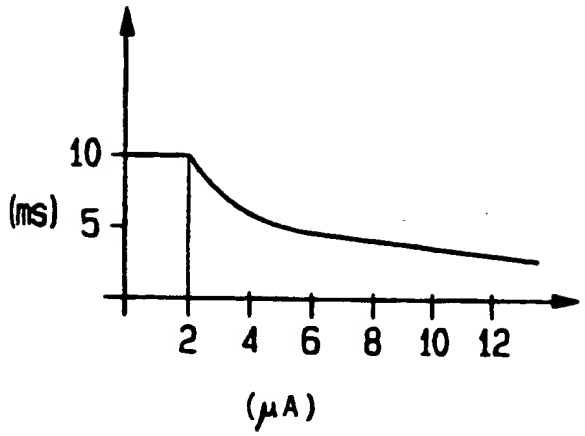

parallel to serial converter
analog buffer
digital buffers
amplifiers
digital control
AGC
sequencer

FIG. 5

FIG.6


10
(ms) 5
2 4 6 8 10 12
(μA)

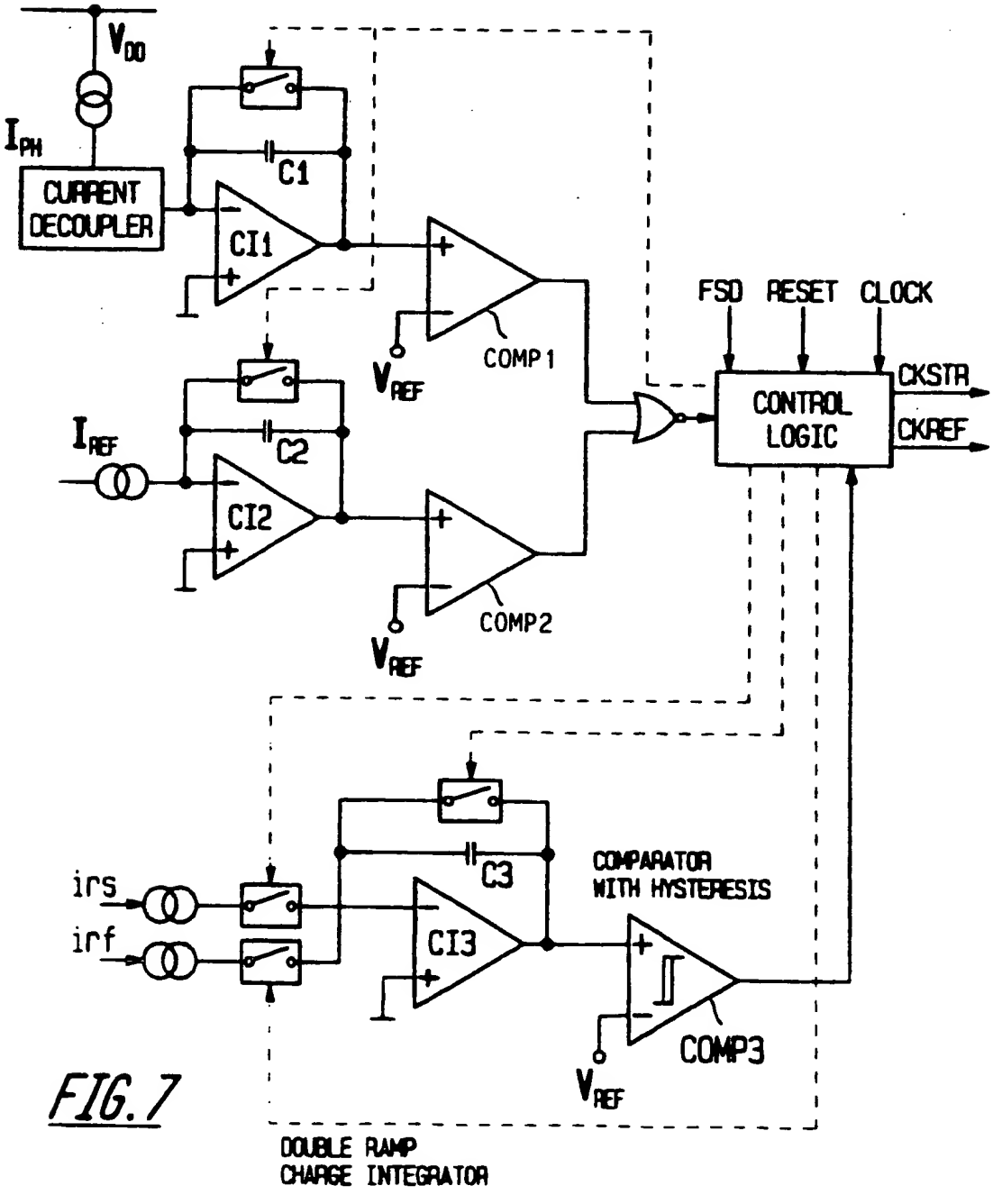

V_{DD}
I_{PH}
CURRENT DECOUPLER
C1
CI1
V_{REF}
COMP1
FSD RESET CLOCK
CONTROL LOGIC
CKSTR
CKREF
I_{REF}
C2
CI2
COMP2
V_{REF}
irs
irf
C3
CI3
COMPARATOR WITH HYSTERESIS
COMP3
V_{REF}
DOUBLE RAMP CHARGE INTEGRATOR

FIG.7

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 83 0485

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP-A-0 630 152 (CANON KK) 21 December 1994 * page 2, line 37 - line 43; claims 1,2,4 * * page 3, line 55 - page 4, line 16; figures 3,9,10 *	1,3-6,8	H04N3/15
A	EP-A-0 616 464 (CANON KK) 21 September 1994		
A	PATENT ABSTRACTS OF JAPAN vol. 007, no. 040 (E-159), 17 February 1983 & JP-A-57 190469 (NIPPON VICTOR KK), 24 November 1982, * abstract *		
			TECHNICAL FIELDS SEARCHED (Int.Cl.6) H04N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	19 April 1996	Montanari, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
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